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Architectural-Level Synthesis Of Asynchronous Systems (1998) The Designer s Guide to VHDL -
Ashenden - 1995 117: The limitations to delay-insensitivity

Patent US9081931 - Cross-coupled transistor

This application is a continuation application under 35 U.S.C. 120 of and so long as the given gate level
feature complies with design rule spacing requirements

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